

Mid-Term Examination

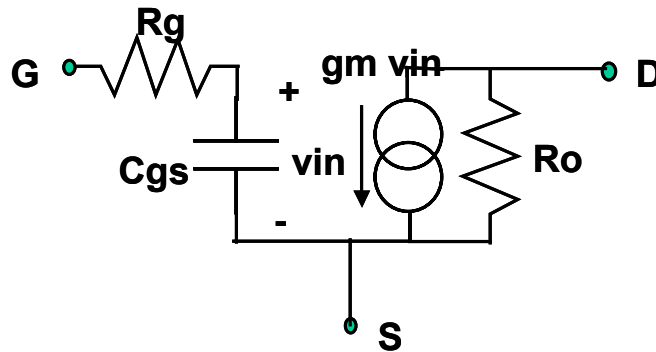
ECE139 Spring 2008

Name.....

General Directions: Answer all four questions. This is a closed book, closed notes examination. There are a few numbers and equations on the back page, for reference. *Numerical answers do not have to be worked out, however; algebraic expressions will do.* Calculators are not allowed in this exam.

Problem 1 (20 points)

Consider a nMOSFET whose small signal model is shown schematically below (at a particular dc operating point at which V_{gs} is above threshold V_t , and V_{ds} high enough to drive the device into saturation).



Consider the device in (standard) common-source operation, as a linear two port network.

- Derive the Y parameters for this network.
- Suppose the device is changed so that the width is made 2x as large as the original device. How do each of the elements of the small signal model change? What are the resulting Y parameters?
- Now the dc operating point is changed for this FET. V_{gs} is increased by 0.5V above what it was previously; V_{ds} is kept the same. How do the resulting Y parameters change?

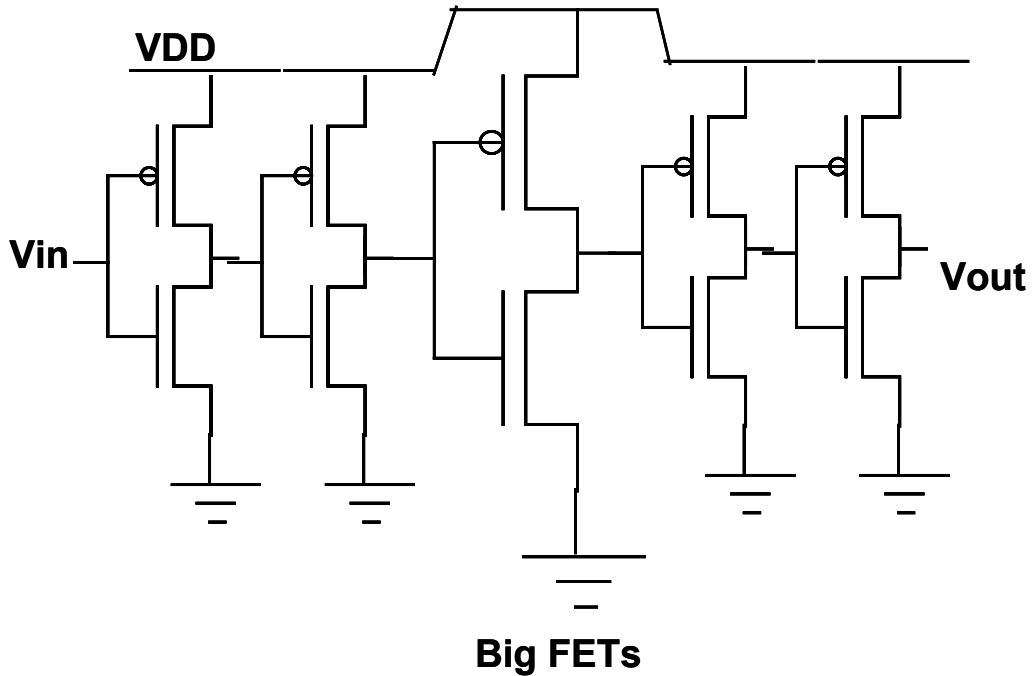
Problem 2 (25 points)

Consider the CMOS inverter chain illustrated below.

The inverter in the center is different from the others. The gate width of both the pFET and of the nFET is larger than that of the others by 4x.

Consider that the inverter chain is driven by a square wave (with finite rise and fall times). Discuss quantitatively how the logic propagation time delay for the center gate (gate #3) differs from the propagation time delay for gate #1 and for gate #2.

What are the physical reasons for the differences in propagation delay?

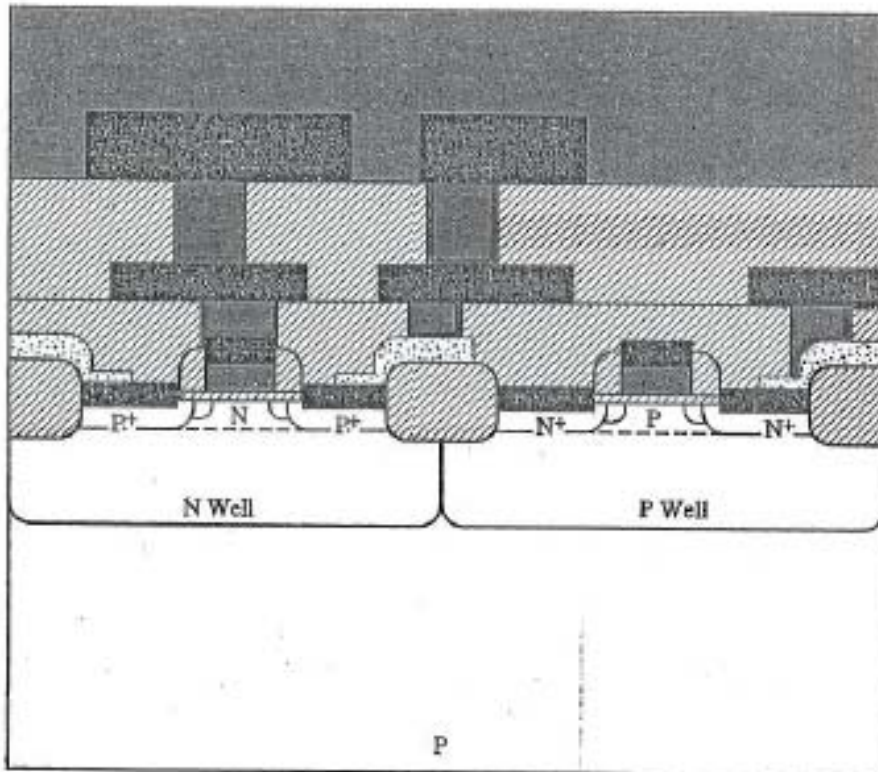


Problem 3 (25 points)

Consider an nMOS structure (made in a CMOS process line) shown in schematic cross-section in the figure below.

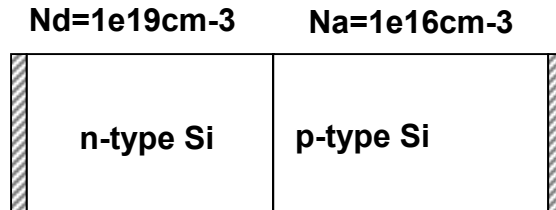
State what process steps you would change in the CMOS process in order to provide the desired outcomes listed below (one change is a sufficient answer for each desired outcome; explain physically why the change should have the desired effect - but you do not have to quantify how much change you need to make).

- a) increase the threshold voltage of the device (by, for example, 0.3V)
- b) increase the f_t of the device (by, for example, 25%)
- c) decrease the width of the lightly doped drain region
- d) thicken the field oxide
- e) reduce the body effect parameter
- f) reduce capacitance associated with interconnect lines connected to the MOSFET

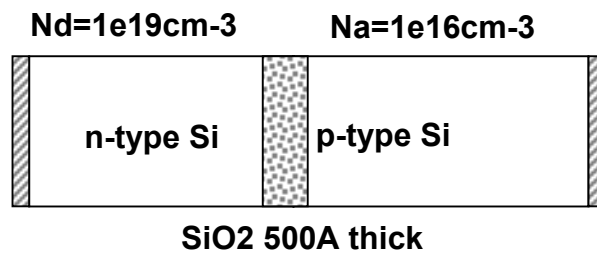


Problem 4 (25 points)

a) Consider the p-n junction fabricated in Si shown below. A reverse bias of 5V is applied to it (the n-side is made +). Draw the band diagram for the structure at the given bias. Please make the drawing approximately to scale (recall the bandgap of Si is about 1.12 eV). Show where the 5V applied voltage appears on the diagram. Estimate how much of the potential variation occurs across the p-doped side of the device (Note the considerable difference in doping levels on the 2 sides).



b) Now consider that a layer of SiO₂ of thickness 500Å is inserted between the n region and the p region, as shown below. The same "reverse" bias voltage of 5V is applied (the n side is made +). For this case, draw the band diagram. Comment on why it looks different from the case above. Estimate how much of the potential variation occurs across the p-doped side of the junction.



Reference numbers and formulas:

$$n_i(\text{Si}, 300\text{K}) = 1.5 \times 10^{10} \text{cm}^{-3}$$

$$N_C(\text{Si}, 300\text{K}) = 2.8 \times 10^{19} \text{cm}^{-3}$$

$$N_V(\text{Si}, 300\text{K}) = 1 \times 10^{19} \text{cm}^{-3}$$

$$E_g(\text{Si}) = 1.12 \text{eV}$$

$$kT(300\text{K}) = 0.026 \text{eV}$$

$$\text{Si relative dielectric constant} = 11.8$$

$$\text{SiO}_2 \text{ relative dielectric constant} = 3.9$$

$$\text{Dielectric constant of free space} = 8.9 \times 10^{-14} \text{ F/cm}$$

Ex: For 300Å thickness, oxide capacitance per unit area is $1.16 \text{ fF}/\mu\text{m}^2$

$$\text{Electron affinity of Si} = 4.1 \text{eV}$$

$$\text{Electron affinity of SiO}_2 = 0.9 \text{eV}$$

$$\text{Bandgap of SiO}_2 = 9 \text{eV}$$

Electron velocity in Si (under doping conditions representative of a FET channel):

$$v = \mu_0 E / (1 + E/E_{\text{sat}})$$

$$\text{with } \mu_0 = 640 \text{ cm}^2/\text{Vsec}$$

$$E_{\text{sat}} = 16000 \text{ V/cm}$$

Hole velocity in Si (under doping conditions representative of a FET channel):

$$v = \mu_0 E / (1 + E/E_{\text{sat}})$$

$$\mu_0 = 240 \text{ cm}^2/\text{Vsec}$$

$$E_{\text{sat}} = 42000 \text{ V/cm}$$

The width w of a one-sided abrupt p-n junction is given implicitly by:

$$V + V_{\text{bi}} = \frac{1}{2} q N w^2 / \epsilon$$

Ex: For $V=1\text{V}$, $\epsilon=11.8 \epsilon_0$, $N=1 \times 10^{16} \text{cm}^{-3}$, the resulting value of w is $0.36 \mu\text{m}$.

Einstein relation for diffusion coefficients: $D / \mu = kT/q$