

ECE 139 Spring 2009

Homework Set #1

Handed out: Apr 2

Due: Apr. 14

Objective: This homework set is intended to provide experience with simple SPICE simulations. Learn to use SPICE as a technique to investigate issues and to answer real questions, not just to generate numbers.

Guidelines for homework (applicable throughout the course)

Solutions should strive to contain the following elements:

- 1) Statement of the problem objective (1 or 2 sentences only)
- 2) Graphical output.
- 3) A description of the conclusions reached, stated clearly in English (1 or 2 sentences).
- 4) Where possible, a comparison of simulated results with an analytical model (which can be crude!!).

The nominal version of SPICE for use in ECE 139 is PSPICE 9.1

The student version of this program is available at no cost from Orcad and other sources which you can find on the web - for example electronics-lab.com. It requires on the order of 30Mb. We will only use the PSPICE A/D portion, with text file input (.cir) rather than schematic input. Various manuals are available on our class website or on the web.

For those who need it, Berkeley SPICE is also available on ACS computers (such as ieng9). To gain access, type "prep spice".

Winspice is a version of Berkeley SPICE that can be downloaded from the web.

SPICE models

SPICE simulations of MOSFETs should be done in relation to some nominal devices. For this set, please use the following (unless otherwise stated).

nMOS

$L = 0.5\mu$ $W = 10\mu$ $\langle AD = 50p$ $AS = 50p$ $PD = 20\mu$ $PS = 20\mu \rangle$ (<these may be omitted for most purposes; if you use them, check units carefully in the SPICE file). A representative input line describing the nFET is

M1 drain gate source body MNLVL1 $L = 0.5\mu$ $W = 10\mu$ (where drain, gate, etc designate the nodes to which the FET is connected).

```
.model MNLVL1 NMOS LEVEL=1
+KP=5e-5 VTO=0.8V GAMMA=0.4
+PHI=0.6 LAMBDA=0.05 RSH=5
+CJ=2e-4 CGSO=2e-10 CGDO=2e-10 TOX=0.025u NSUB=1e16
```

pMOS

$L = 0.5\mu$ $W = 25\mu$ $\langle AD = 125p$ $AS = 125p$ $PD = 50\mu$ $PS = 50\mu \rangle$

```
.model MNLVL1 PMOS LEVEL=1
```

```
+KP=2e-5 VTO=-0.8V GAMMA=0.4
+PHI=0.6 LAMBDA=0.05 RSH=5
+CJ=2e-4 CGSo=2e-10 CGD0=2e-10 TOX=0.025u NSUB=1e16
```

Problem 1

Use SPICE to calculate and plot the dc I-V characteristics of an n-channel MOSFET, as follows:

- Plot I_D vs V_{DS} at various gate bias values V_{GS} (and body tied to the source). Sweep V_{DS} from 0 to 4 V. Pick values up to +4V for V_{GS} , and include values of V_{GS} low enough to go below threshold.
- Determine the source-drain resistance of the FET (dI_{DS}/dV_{DS}) at $V_{DS}=0$, vs V_{GS} . Compare this with expectations from theory. You may not be able to plot this directly in PSPICE, use a tool of your choice (or a hand plot).
- Plot I_D vs V_{GS} for drain biases in the saturation regime (pick $V_{DS}=4V$ for simplicity).
- Plot the transconductance g_m of the n-channel MOSFETs (at a particular V_{DS} , say $V_{DS}=4V$, in the saturation regime $V_{DS}>V_{GS}-V_T$) vs V_{GS} .
- What happens to the transconductance of the transistor at a given bias condition (V_{GS} , V_{DS}) when the width of the transistor is increased by a factor of 2 (going from 10 μ m to 20 μ m)? What happens to the drain-source resistance (when the device is fully on, near $V_{ds}=0$)?

Problem 2

Contrast the behavior calculated in Problem 1, with that which you obtain with a more exact representation of a MOSFET. Use the following BSIM3 model (PSPICE level 6)

```
.model MNLVL6 NMOS level=6
+tox=2e-8 xj=1.5e-7 npeak=1.7e17 nsub=3e16
+u0=670 vsat=8e6 ua=2e-9 ub=6e-19 uc=0.04
+vth0=0.8 k3=80
+pclm=1.3 pdibl1=0.39 pdibl2=0.0086
+dROUT=0.6 dvt0=3 dvt1=0.5 dvt2=-0.05
+subthmod=2 nfactor=1
+cj=2e-4 cgso=2e-10 cgbo=2e-10
```

(save this model file for later use in ECE139)

- Recompute the plot of I_D vs V_{DS} with V_{GS} as a parameter. Compare with the plot of Problem 1, and comment on the differences you see. You can overlay the plots by using a command available under the file menu of Probe.
- Recompute the plot of I_D vs V_{GS} at $V_{DS}=4V$. Compare with Problem 1, and once again comment on the differences.
- It is frequently important in circuit design to have a high value of transconductance. It is also important to have low power dissipation, which corresponds to having a low I_D . Compare the plots of I_D and of g_m vs V_{GS} (keeping constant $V_{DS}=4V$ for simplicity), and decide what bias condition provides the best tradeoff. Hint: consider plotting I_D and g_m on a log scale and/or plotting g_m/I_D . If you use the bias condition you identified, and you need to reach a specific value of g_m in your circuit (say, $g_m=20mS$),

what device size should you pick? What considerations can you think of that might also influence your choice?

Problem 3

Consider the device of Problem 1 connected in the following simple circuit. There is a voltage source connected to the gate, with dc value V_{GS} , and ac value =1. Similarly, the drain is connected to a voltage source with dc value V_{DS} . The source is grounded, as is the body.

Pick a representative value of V_{GS} (say 4V) and V_{DS} (say 4V) and carry out an ac analysis, over the range 1MHz to 10GHz, for example.

a. Determine the ac input current as a function of frequency. What is its phase relative to the input voltage?

b. Determine the small signal input impedance(=ac input voltage/ac input current) as a function of frequency. Note this is a complex number. Does this correspond to the impedance of a capacitor, inductor, resistor or other circuit combination? What is the value of the appropriate circuit model element? Compare with what you expect, given the area of the gate, and the gate oxide thickness. You can use simple expressions for the capacitance of a parallel plate capacitor.

c. Determine the output ac current vs frequency. What is its phase relative to the input current and voltage?

d. Plot the magnitude of the current gain (ie magnitude of ac output current divided by ac input current) vs frequency. What is the ft of the device (where ft is defined to be the frequency at which the current gain -into an ac short circuit - drops to magnitude of unity)?

e. Determine an estimate of the transconductance g_m by computing the magnitude of the ac output current divided by the ac input voltage. Does this transconductance agree with that determined in Problem 1 (for the $V_{GS}=4V$, $V_{DS}=4V$ condition)?

f. What is the relationship between the values of transconductance, input capacitance and ft that you have determined?

g. Now include a resistor of value 50 ohms between the drain of the transistor and the power supply. Increase the value of V_{dd} so that the device dc drain voltage remains 4V. Recompute the current gain as a function of frequency. Has the value changed from the result you got earlier? If so why?

h. Reconfigure the circuit so that you can use ac analysis to determine the Y parameters Y_{12} and Y_{22} .

i. Use your results to determine the effect value of R_o and C_{dg} for the transistor.

