

ECE 139 Spring 2009 Homework Set #1 Solutions

Objective: This homework set is intended to provide experience with simple SPICE simulations. Learn to use SPICE as a technique to investigate issues and to answer real questions, not just to generate numbers.

SPICE models

SPICE simulations of MOSFETs should be done in relation to some nominal devices. For this set, please use the following (unless otherwise stated).

nMOS

$L = 0.5\mu$ $W = 10\mu$ $\langle AD = 50p$ $AS = 50p$ $PD = 20u$ $PS = 20u \rangle$ (<these may be omitted for most purposes; if you use them, check units carefully in the SPICE file). A representative input line describing the nFET is

M1 drain gate source body MNLVL1 L=0.5u W=10u (where drain, gate, etc designate the nodes to which the FET is connected).

```
.model MNLVL1 NMOS LEVEL=1
+KP=5e-5 VTO=0.8V GAMMA=0.4
+PHI=0.6 LAMBDA=0.05 RSH=5
+CJ=2e-4 CGSO=2e-10 CGDO=2e-10 TOX=0.025u NSUB=1e16
```

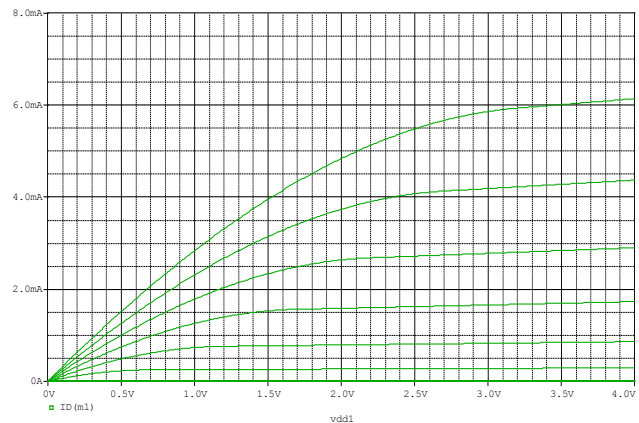
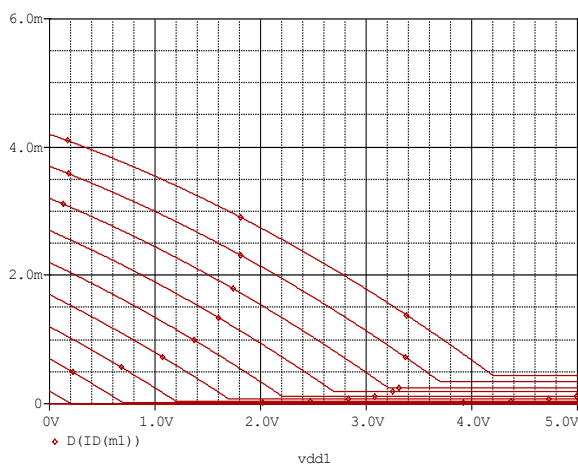
pMOS

$L = 0.5\mu$ $W = 25\mu$ $\langle AD = 125p$ $AS = 125p$ $PD = 50u$ $PS = 50u \rangle$

```
.model MNLVL1 PMOS LEVEL=1
+KP=2e-5 VTO=-0.8V GAMMA=0.4
+PHI=0.6 LAMBDA=0.05 RSH=5
+CJ=2e-4 CGSO=2e-10 CGDO=2e-10
TOX=0.025u NSUB=1e16
```

Problem 1

Use SPICE to calculate and plot the dc characteristic of an n-channel MOSFET, as follows:



a. Plot I_D vs V_{DS} at various gate bias values V_{GS} . The plot shows I_{ds} for V_{gs} ranging from 0 to 4V in 0.5V steps.

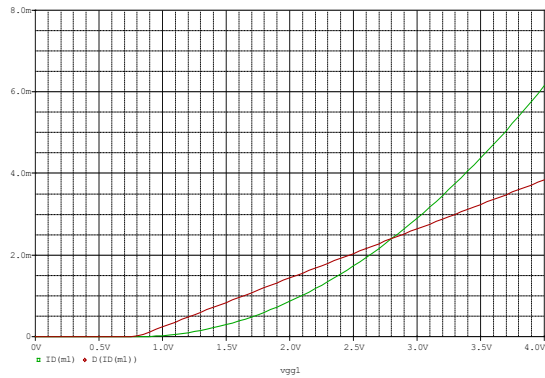
b. Determine the source-drain resistance of the FET at $V_{DS} = 0$, vs V_{GS} . Compare this with expectations from theory.

With the $D(I_D)$ function we can easily get dI_D/dV_{DS} vs V_{DS} . The values of R_{sd} are $1/D(I_D)$ values plotted here.

We expect to find $R_{ds} = [C_{ox}\mu(V_{gs} - V_t)W/L]^{-1}$ in this regime. Using

$C_{ox} = \epsilon_{ox}/t_{ox} = 1.39e-7 F/cm^2$, and guessing $\mu = 400 cm^2/Vsec$, we find $R_{ds} = 214 \text{ ohms}$ ($1/R_{ds} = 4.7e-3 S$) for $V_{gs} = 5V$, in good agreement with the plot (reading the value at $V_{ds} = 0V$).

c. Plot I_D vs V_{GS} for drain biases in the saturation regime (pick $V_{DS} = 4V$ for simplicity).



d. Plot the transconductance g_m of the n-channel MOSFETs (at a particular V_{DS} , say $V_{DS} = 4V$, in the saturation regime $V_{DS} > V_{GS} - V_T$) vs V_{GS} .

Plot on left shows I_d vs V_{gs} and g_m vs V_{gs} (obtained by $D(I_d)$ when I_d is plotted vs V_{gs}).

e. What happens to the transconductance of the transistor at a given bias condition (V_{GS} , V_{DS}) when the width of the transistor is increased by a factor of 2 (going from $10\mu m$ to $20\mu m$)? What happens to the source drain

resistance? Doubling width of transistor increases g_m by $x2$, and decreases R_{ds} by $x2$ (equivalent to placing two transistors in parallel)

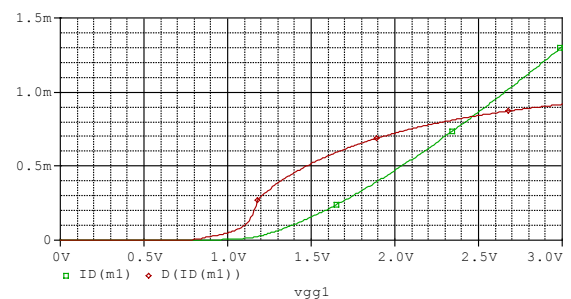
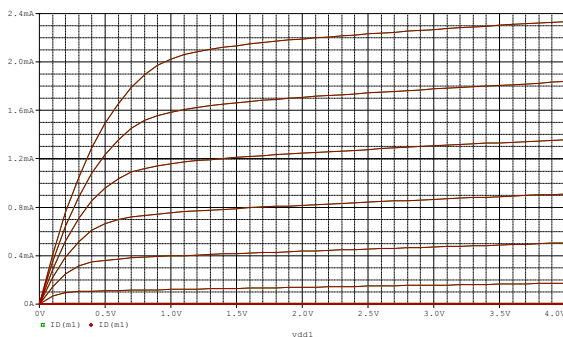
Problem 2

Contrast the behavior calculated in Problem 1, with that which you obtain with a more exact representation of a MOSFET. Use the following BSIM3 model (PSPICE level 6)

```
.model MNLVL6 NMOS level=6
+tox=2e-8 xj=1.5e-7 npeak=1.7e17 nsub=3e16
+u0=670 vsat=8e6 ua=2e-9 ub=6e-19 uc=0.04
+vth0=0.8 k3=80
+pclm=1.3 pdibl1=0.39 pdibl2=0.0086
+dROUT=0.6 dvt0=3 dvt1=0.5 dvt2=-0.05
+subthmod=2 nfactor=1
+cj=2e-4 cgso=2e-10 cgbo=2e-10
```

(save this model file for later use in ECE139)

a. Recompute the plot of I_D vs V_{DS} with V_{GS} as a parameter. Compare with the plot of



Problem 1, and comment on the differences you see.

b. Recompute the plot of I_D vs V_{GS} at $V_{DS}=4V$. Compare with Problem 1, and once again comment on the differences.

Representative values are shown above. With the level 6 model, the current is smaller, the knee voltage is smaller, the current varies linearly with V_{GS} (the g_m value tends to saturate at high V_{GS}).

Problem 2

Consider the device of Problem 1 connected in the following simple circuit. There is a voltage source connected to the gate, with dc value V_{GS} , and ac value $=1$. Similarly, the drain is connected to a voltage source with dc value V_{DS} . The source is grounded.

a. Pick a representative value of V_{GS} (say 4V) and V_{DS} (say 4V).

Determine the ac input current as a function of frequency. What is its phase relative to the input voltage?

$I_{in}=I_g$ is shown here on log-log scale. Phase is 90 degrees shifted with respect to voltage (input current phase leads the voltage).

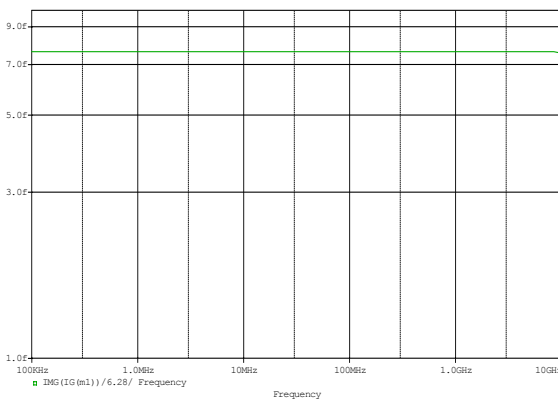
b. Determine the small signal input impedance. Does this correspond to that of a capacitor, inductor, resistor or other circuit combination? What is the value of the appropriate circuit model element? Compare with what you expect, given the area of the gate, and the gate oxide thickness.

Input impedance follows $1/\omega$, with 90 degree shift; this corresponds to a capacitor. Value is found to be $C_{in}=7.9e-15 F$.

The plot on the left shows $I_g/2\pi/\text{frequency}$. It is constant= $7.9e-15 F$.

c. Determine the output ac current vs frequency. What is its phase relative to the input current and voltage?

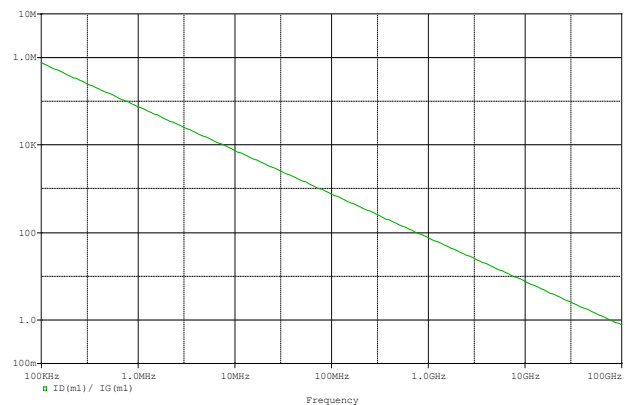
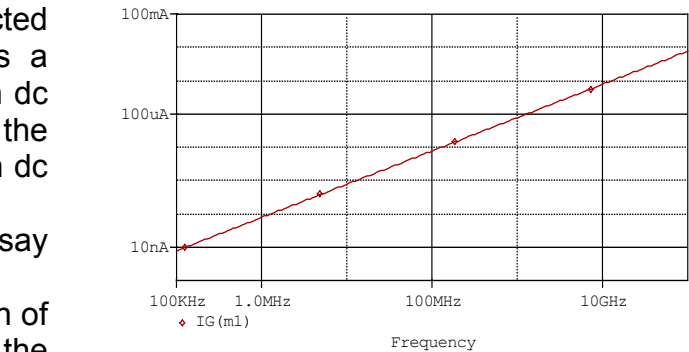
Output current is in phase with input



voltage, 90 degrees shifted with respect to input current.

d. Plot the magnitude of the current gain (ie ac output current divided by ac input current) vs frequency. What is the ft of the device?

From the plot at the right ft is about 70GHz (a little larger than the range suggested in the problem set).



e. Determine the magnitude of the ac output current divided by the ac input voltage. Does this transconductance agree with that determined in Problem 1? *The plot below shows that the ac determined $g_m = \Delta I_D / \Delta V_G$ is about constant = 3.9×10^{-3} S. This matches the value found in the dc plots.*

f. What is the relationship between the values of transconductance, input capacitance and f_t that you have determined? *The results confirm that $f_t = g_m / (2\pi C_{in})$*

