

ECE139 Spring 2009 Problem Set #2

Handed out: Apr. 14

Due date: Apr. 23

Objective: This homework set is intended to provide more experience with simple SPICE simulations, highlighting the relationship between device performance and model parameters. Microwind is also used to highlight the relationship between device layout and circuit.

Software: Download the Microwind2 zipfile from the class web-site, ece-classweb.ucsd.edu/~ECE139. This zipfile includes an on-line brief manual, along with the executable program and numerous examples. A lengthier pdf manual is also available for download, but may not be required to complete the homework.

SPICE Models (similar to problem set 1, some dimensions changed)

nMOS

L=0.5um W=3um <AD=9um² AS=9um² PD=9um PS=9um NRD=0.2 NRS=0.2>
(<these may be omitted for most purposes; if you use them, check units carefully in the spice file>)

```
.model MNLVL1 nmos (LEVEL=1  
+KP=5e-5 VTO=0.6V GAMMA=0.4  
+PHI=0.6 LAMBDA=0.05 RSH=5  
+CJ=2e-4 CGSo=2e-10 CGDo=2e-10 TOX=0.015U NSUB=1e16)
```

pMOS

L=0.5um W=5um <AD=27um² AS=27um² PD=15um PS=15um NRD=0.2 NRS=0.2>

```
.model plvl1 pmos (LEVEL=1  
+KP=2e-5 VTO=-0.6V GAMMA=0.4  
+PHI=0.6 LAMBDA=0.05 RSH=5  
+CJ=2e-4 CGSo=2e-10 CGDo=2e-10 TOX=0.015U NSUB=1e16)
```

Problem 1

a) Model a simple CMOS inverter using SPICE, using a power supply voltage $V_{dd}=3V$. Compute and plot the dc transfer curve: v_{out} vs v_{in} on a dc basis. What is the "switching voltage"?

b) Show how the "switching voltage" varies as KW/L for the pull-up is made different from that of the pull-down FET. You can do this by changing dimensions in the spice models above as needed. Decide on appropriate sizes for the two transistors in order for the "switching voltage" to be $V_{DD}/2$.

Problem 2

a) Determine the switching speed for the inverter circuit of problem 2.1, with fan-out of unity, along with a wiring capacitance of 50fF. In order to do this, make up an overall circuit with 4 identical inverters (each one having 50fF to ground connected to its output).

Drive the first inverter with a periodic pulse waveform with representative values (say, 0 to 3V, 50PS rise and fall times, at 200MHz repetition rate; adjust these values if necessary). Plot the transient behavior of the outputs of the 4 inverters of this chain. Then measure the "switching delay time" of the 3rd inverter. This "switching delay time" is the delay time between the input waveform at the midpoint of its swing, and the corresponding point on the output waveform. Look at different sections of your time response to see if the delay time for rising input is the same as the delay time for falling input. Determine the average value of these two values. [The use of a long inverter chain in the simulation is to make sure that the waveforms used in the analysis are proper. The middle stages see input waveforms that are different from the arbitrarily assumed input waveform].

b) Examine the drain current waveforms from a representative gate (pick number 3 in the delay chain you made). How much current is delivered to the load as a function of time? Show that the net load current averages to zero. You may use the S(f(t)) function within PSPICE's Probe menu, which finds the integral of the waveform f(t). How much charge is delivered to the load during the pull up phase of each switching cycle? Does this result make sense? How much current is drawn from the VDD supply that does not go to the load? (this current is sometimes referred to as "shoot-through current" or "crowbar current").

c) Place extra capacitances at the output nodes of the inverters, and repeat the gate delay determination. By finding the delay for several capacitances, determine the delay equation for the technology. What is the value of R_{seff}, the effective source resistance of the CMOS switch? Comment on how this value together with the observed capacitance for a single stage can be used to predict the gate delay.

Problem 3

Use the Microwind program to simulate an inverter as follows. Set the technology file to correspond to 0.25um CMOS. Use the default gate oxide thickness and gate length values for this file. Layout a simple CMOS inverter (of your own design). Use the Design Rule checker to verify that no design rules are violated. Choose gate widths for pull-down and pull-up devices that will give approximately symmetric transient responses. Place a clock voltage source at the input of the inverter, and assign VDD and VSS connections. Be sure to connect the n-well to the positive supply voltage.

a) Simulate the structure in the time domain to verify functionality.

b) Use the voltage vs voltage plot to determine the logic transfer voltage for your inverter. At what input voltage does the gate switch state?

c) Investigate the "simulate on layout" capability to view the operation of the inverter.

Problem 4

Use copy and paste provisions to layout a structure containing 5 inverters in sequence. Use the Design Rule Checker to determine that the design is legal. Once again, place a clock voltage source at the input of the delay chain, assign VDD and VSS connections, and be sure to connect the n-well to the positive supply voltage.

a) Simulate the structure in the time domain, and determine the propagation delay for your inverter (the one in the middle) by examining the sequence of output waveforms. For this and subsequent simulations, the Level 1 model may be used.

b) Determine the capacitance of the output node of the center inverter by examining the characteristics of the node. What contributes to this capacitance?

c) Determine the spice netlist for your inverter chain. Observe the capacitance assigned to the output node you have previously examined. Does this value make sense?