ECE139 Spring 2009
Problem Set #4

Handed Out: May 14 Due date: May 26

Guidelines: As usual, the homework writeup should include some comments on the results, including conclusions, back-of-the-envelope (or napkin) analyses, discussion of physical mechanisms, etc.
This problem set deals with MOSFET simulations with Silvaco software.
For simplicity, the Silvaco problems are closely related to the Silvaco file template mostest.in.

- *Login to ieng9 or ee3327-10, 11, 12...*
- *Type prep ee139s, this provides path entries to our course*
- *In directory ee139s/public, find mostest.in; copy it to your directory*
- *Type prep silvaco, this provides path entries to the silvaco software*
- *Type deckbuild &, this starts silvaco menu driven control program.*
- *After modifying and executing your programs, type tonyplot &, this starts the silvaco plotting program in order to view the results.*

The sequence of drain and gate voltages that are requested in the program are important for convergence.

Problem 1
Simulate the electrical characteristics of an n-channel MOS transistor, using the Silvaco program Atlas, according to the device listing provided (mostest.in). Note that the gate length is 1um.
(a) Consider first a bias condition of Vs=0, Vsubstrate=0, Vd=+0, Vg=2V; this makes the channel relatively uniform across the device, and should yield results comparable to the 1 dimensional approximations. Plot the characteristics of the channel by making a vertical cutline through the gate oxide, channel and substrate near the midpoint of the device. Plot n and p vs depth; separately, plot electric field and electrostatic potential. Finally, plot band conduction and valence band energy. Comment on whether the values agree with your expectations from simple analysis. You may need to verify the doping density near the surface.
(b) Now consider the bias condition of Vs=0, Vsubstrate=-2V, Vd=0, Vg=2V. Plot the electric field and electrostatic potential vs depth, and comment on differences with part a.
(c) With Vsubstrate=0V again, compute the structure for Vs=0, Vg=2V and Vd=+3V. Make vertical cutlines at the source side of the channel, the midpoint of the channel and at the drain side of the channel, plotting n,p; E field and potential; and band diagram. Comment on the differences between them, and the relationship with the diagrams of part a.

Problem 2
For the case of the 1um gate length FET, use Silvaco to calculate the lateral electric field (in the direction of the current flow) as a function of position going from the source to the drain. Plot this for the depth corresponding to the very top of the inversion channel, next to the oxide. Consider one specific bias condition: VGS=+2V, VDS=+3V.
Explain the shape of the plot. Does the value of the electric field near the source agree with expectations?

Mark on your plot the region where you might expect velocity saturation to occur.

Problem 3
Use Silvaco to calculate Ids vs Vgs and gm vs Vgs for FETs with gate length 1um. Use Vds=4V and plot for Vgs from 0 to 4V. You may want to find gm by numerical differentiation, not by using Silvaco. How do the results compare with gradual channel approximation, and with saturated velocity approximation?

Problem 4
Determine the subthreshold current for the nominal nMOS device that you studied in Problem 1, with gate length 1um. Plot log(Ids) vs Vgs. (Pick a range of Vgs that extends below and above the nominal threshold). Calculate the corresponding "subthreshold slope" (in mV/decade). How does the resulting value compare with expectations?

Problem 5
Use Silvaco to calculate Ids vs Vgs for the gate length of 1um, with larger values of Vds than 4V (try several of them). Determine how the threshold voltage changes with Vds (this corresponds to the "drain-induced barrier lowering" DIBL effect). To determine the threshold, consider the value of Vgs where the current per unit gate width reaches Id=10^{-7}A/um.